Abstract f the Discl sure

There is an SRAM which can perform a high-speed read operation at a low power supply voltage and which can simplify a circuit configuration and manufacturing steps. When signals at levels "H" and "L" are output from a flip-flop to storage nodes, respectively, the threshold voltages of first and second N-channel MOS transistors having channel regions connected to the storage node decrease to improve the current drive capabilities of the transistors. The second N-channel MOS transistor is set in an ON state by the level of the storage node. In this case, when a word line goes to level "H", the first N-channel MOS transistor is turned on, and a bit line is drawn in a ground potential at a high speed.